REMARKS

Claims 34-37, 46 and 53-58 are pending in the present application. Claims 34 and 53 have been amended. Claims 38, 45 and 47 have been canceled.

Information Disclosure Statement

An Information Disclosure Statement has been filed on April 27, 2007, in connection with this application. The Information Disclosure Statement and corresponding references submitted therewith have been entered into the image file wrapper of this application on the U.S. Patent Office website. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the documents submitted therewith have been considered and will be cited of record in the present application.**

Specification

The abstract of the disclosure has been objected to as allegedly including reference characters. However, the abstract as amended on pages 9-10 of the Preliminary Amendment dated September 9, 2003, does not include reference characters. Correction of the abstract as requested is therefore unnecessary. The Examiner is therefore respectfully requested to withdraw the objection to the abstract.

Claim Objections

Claims 34 and 53 have been objected to in view of the informalities as listed on page 2 of the current Office Action dated March 7, 2007. Claims 34 and 53 have been corrected as requested. The Examiner is therefore respectfully requested to withdraw the objection to the claims.

Double Patenting Rejection

Claims 34-37 and 53-57 have been provisionally rejected on the grounds of non-statutory obviousness-type double patenting as being unpatentable over claims 24-27 and 29-33 of copending application Serial No. 11/077,145. This rejection is respectfully traversed for the following reasons.

Claim 34 has been amended to include the features of dependent claim 38. Claim 53 has been amended in a somewhat similar manner. Accordingly, the provisional rejection on the grounds of non-statutory obviousness-type double patenting should no longer be applicable to the above noted claims. The Examiner is therefore respectfully requested to withdraw the provisional obviousness-type double patenting rejection for at least these reasons.

Claim Rejections-35 U.S.C. 102

Claims 34-38 and 46 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Lin et al. reference (U.S. Patent No. 5,239,198). This rejection,

insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Claim 34 has been amended to include in combination the features of dependent claim 45. Applicants therefore respectfully submit that the semiconductor device of claim 34 distinguishes over the Lin et al. reference as relied upon and that this rejection, insofar as it may pertain to claims 34-37 and 46, is improper for at least these reasons.

With further regard to this rejection, as emphasized beginning on page 9 of the Amendment dated June 29, 2006, passive electronic component 50 of the Lin et al. reference is not described or even remotely suggested as being "a semiconductor chip", as asserted by the Examiner. As described in column 6, lines 61-64 of the Lin et al. reference: "As illustrated in FIG. 6, a passive electronic component 50, such as a resistor, diode, decoupling capacitor, or the like, is electrically coupled to conductive traces 16 by solder joints".

Accordingly, passive electronic component 50 in Figs. 6 and 7 of the Lin et al. reference is merely a resistor, a diode, a decoupling capacitor, **or the like**. That is, passive electronic component 50 of the Lin et al. reference is a single electronic component that does not need to be overmolded with encapsulant. There is no description in the Lin et al. reference characterizing passive electronic component 50 as "a semiconductor chip". It should thus be clear that passive electronic component 50 of the Lin et al. reference is not a CSP type semiconductor device as would be understood

by one of ordinary skill. Particularly, CSP type semiconductor devices are understood to be devices that are capable of realizing various sophisticated functions, and are not merely a resistor, a diode, a capacitor, or the like. The Examiner's attention is again directed to the excerpt of the Wolf et al. text (Silicon Processing for the VLSI Era, Vol. 1: Process Technology) as enclosed along with the Amendment dated August 9, 2005, which describes and illustrates a CSP type semiconductor device as would be understood by one of ordinary skill.

In the current Office Action dated March 7, 2007, the Examiner has failed to address the above noted traversal of the rejection in view of the Lin et al. reference. It would appear that the Examiner has completely ignored the arguments of record as submitted by Applicants. ***Again, the Examiner is requested to identify in the Lin et al. reference explicit description of passive electronic component 50 as "a semiconductor chip", and how passive electronic component 50 may be interpreted as a CSP type semiconductor device as would be understood by one of ordinary skill.***

Applicants respectfully submit that the Lin et al. reference does not disclose a CSP type semiconductor device mounted on an area of a backside surface of a base plate of a BGA type semiconductor device, as would be necessary to meet the features of claim 34. Accordingly, Applicants respectfully submit that the semiconductor device of claim 34 distinguishes over the Lin et al. reference as relied upon, and that this rejection, insofar as it may pertain to claims 34-37 and 46, is improper for at least these

additional reasons.

Claim Rejections-35 U.S.C. 103

Claims 45, 47 and 53-56 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference in view of the Okuno et al. reference (U.S. Patent No. 6,063,646). This rejection is respectfully traversed for the following reasons.

Applicants respectfully submit that the Examiner's reliance upon the Lin et al. reference is improper for at least the reasons as set forth above. Particularly, the Lin et al. reference does not disclose a CSP type semiconductor device mounted on the backside surface of a base plate of a BGA type semiconductor device.

With further regard to this rejection, the Examiner has secondarily relied upon the Okuno et al. reference as disclosing a CSP type semiconductor device. However, the Examiner has established no motivation for modifying the structure shown in Figs. 6 and 7 of the Lin et al. reference to include a CSP type semiconductor device in place of passive electronic component 50 such as a resistor, diode, decoupling capacitor, or the like. The prior art as relied upon does not provide a high-performance semiconductor device utilizing the functions of two different semiconductor device types (BGA and CSP). That is, the prior art as relied upon does not teach the use of such semiconductor device types in combination so as to prevent size increase, while at the same time enabling various sophisticated functions. Moreover, the relied upon prior art does not disclose a backside surface of a base plate of a BGA type semiconductor

device, with a CSP type semiconductor device mounted on a backside surface of the base plate of the BGA type semiconductor device and wherein the CSP type semiconductor device has a thickness less than a thickness of a plurality of bumps formed on the base plate. Accordingly, Applicant respectfully submits that claims 45 and 47 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

The semiconductor device of claim 53 includes in combination among other features that "the backside surface of the base plate is mounted to a printed circuit board via the plurality of bumps, and said CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps". Applicants respectfully submit that for at least somewhat similar reasons as set forth above, the semiconductor device of claim 53 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 53-56 is improper for at least these reasons.

Claims 34, 37, 45-47, 57 and 58 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Inaba et al. reference (U.S. Patent No. 6,166,443) in view of the Okuna et al. reference. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

As noted above, claim 34 has been amended to include the features of dependent claim 38. Applicants therefore respectfully submit that claim 34 would not

have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 34, 37, 46, 57 and 58, is improper for at least these reasons.

Conclusion

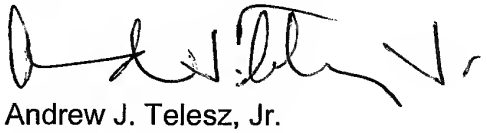
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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